

### **REMARKS**

New claims 61-75 are added. Claims 36-75 are pending in the application.

Claims 36-60 stand rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which allegedly was not described in the specification.

The Examiner is respectfully reminded that MPEP §2163 I. (8th Edition) states it is now well accepted that a satisfactory description may be in the claims or any other portion of the originally-filed specification and an applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, **figures**, diagrams, and formulas that fully set forth the claimed invention (citations omitted).

Regarding the §112 rejection against claims 36-45, the Examiner alleges that a source or drain region elevationally above the channel region and one of the regions to have a portion thicker than the channel region is not disclosed (Page 2 of Paper No. 8). Independent claim 36 recites one of a source region or a drain region elevationally above a channel region, the one region comprising at least a portion thicker than the channel region. Support for the limitation is clearly shown, by Figs. 5-6 and 11. For example, Fig. 5 discloses an exemplary source/drain region 32 elevationally above channel region 31 and over the illustrated substrate 12. The illustrated dimension of the source/drain region 32 in the x-axis direction is clearly shown as being greater than either of the two dimensions shown of the source/drain region 13. Accordingly, at least a portion of source/drain region 32 is **thick** r than channel region 31. The recitation of claim 36 to one region comprising

at least a portion thicker than the channel region is clearly supported by the originally-filed application, and therefore, the §112 rejection is inappropriate and should be withdrawn.

Moreover, since the §112, first paragraph rejection against claims 36-45 is the only rejection presented against such claims, claims 36-45 are now allowable. Applicant respectfully requests allowance of claims 36-45 in the next office action.

Regarding the §112, first paragraph rejection against claims 46-55, the Examiner alleges that a second thin film source/drain region where the first source/drain region has a different thickness than the second source/drain region is not disclosed (Page 2-3 of Paper No. 8). Claim 46 recites a first S/D region having a different thickness than the second S/D region. Support for such limitation is clearly shown, for example, by Figs. 5-6 and 11 of the originally-filed application. For example, Fig. 5 discloses an exemplary S/D region 32 and another exemplary S/D region 13. The illustrated two dimensions of the S/D region 32 (in x and y directions) are clearly shown as being greater than either of the two dimensions shown of the S/D region 13. Accordingly, a first S/D region having a different thickness than the second S/D region is clearly shown, and therefore, the limitation recited in claim 46 is supported by the originally-filed application. The §112, first paragraph rejection against claims 46-55 is inappropriate and should be withdrawn. Moreover, since this is the only rejection presented against claims 46-55, such claims are allowable. Applicant respectfully requests allowance of claims 46-55 in the next office action.

Regarding the §112, first paragraph rejection against claims 56-60, the Examiner alleges that an annulus having a top disposed elevationally below the upper surface, and a first and second diffusion region disposed over the upper surface are not disclosed (Page 3 of Paper No. 8). Claim 56 recites a second dielectric layer having an upper surface, a gate dielectric layer disposed over a portion of the sidewalls as an annulus, and the annulus having a top disposed elevationally below the upper surface. Support for such limitations are clearly shown in Fig. 11. An exemplary gate dielectric layer annulus 26b is shown having a top disposed elevationally below the upper surface of second dielectric layer 18. Accordingly, the recitation by claim 56 to the annulus having a top disposed elevationally below the upper surface is supported by the originally-filed application.

Moreover, the other claim limitation allegedly not supported, that is, a first and second diffusion region disposed over the upper surface, is not recited in any of the claims. Respectfully, the Examiner will note that claims 57-58 and 60 recite to one of a first diffusion region and a second diffusion region disposed over the upper surface. Such limitation of claims 57-58 and 60 is clearly shown, for example, at Figs. 5-6 and 11.


The §112, first paragraph rejection against claims 56-60 is inappropriate and should be withdrawn. Moreover, since this is the only rejection presented against claims 56-60, such claims are allowable. Applicant respectfully requests allowance of claims 56-60 in the next office action.

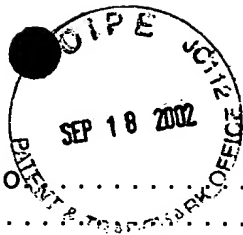
Further, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed together with this application on August 1, 2001. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 9-18-02

By:   
D. Brent Kenady  
Reg. No. 40,045



Application Serial No. .... 09/920,979  
Filing Date ..... August 1, 2001  
Inventor ..... Monte Manning  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2822  
Examiner ..... Kiesha L. Rose  
Attorney's Docket No. .... MI22-1698  
Title: Thin Film Transistors and Methods of Forming Thin Film Transistors

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING  
RESPONSE TO JUNE 28, 2002 OFFICE ACTION

**In the Claims**

The claims have been amended as follows. Underlines indicate insertions  
and ~~strikeouts~~ indicate deletions.

There are no amendments to the claims.

**New Claims**

61. (New) The thin film transistor of Claim 36, wherein the channel region  
comprises an annulus.

62. (New) The thin film transistor of Claim 36, wherein the channel region  
extends from immediately adjacent the substrate.

63. (New) The thin film transistor of Claim 36, wherein the channel region defines an opening.

64. (New) The thin film transistor of Claim 36, wherein the channel region defines an opening between the source region and the drain region.

65. (New) The thin film transistor of Claim 36, wherein the channel region is formed over the gate and defines an opening within the gate.

66. (New) The thin film transistor of Claim 46, wherein the thin film channel region comprises an annulus.

67. (New) The thin film transistor of Claim 46, wherein the thin film channel region extends from immediately adjacent the substrate.

68. (New) The thin film transistor of Claim 46, wherein the thin film channel region defines an opening.

69. (New) The thin film transistor of Claim 46, wherein the thin film channel region defines an opening between the first S/D region and the second S/D region.

70. (New) The thin film transistor of Claim 46, wherein the thin film channel region is formed over the gate and defines an opening within the gate.

71. (New) The thin film transistor of Claim 56, wherein the channel region comprises an annulus.

72. (New) The thin film transistor of Claim 56, wherein the channel region extends from immediately adjacent the substrate.

73. (New) The thin film transistor of Claim 56, wherein the channel region defines an opening.

74. (New) The thin film transistor of Claim 56, wherein the channel region defines an opening between the sidewalls.

75. (New) The thin film transistor of Claim 56, wherein the channel region is formed over the gate dielectric layer and defines an opening within the gate dielectric layer.

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